

# Circuits logiques programmables

- Circuits CPLD
- Circuits FPGA

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## Programmable Logic Devices (PLD)

circuit monolithique formé de cellules logiques (comportant des fusibles, des antifusibles ou de la mémoire) qui peut être programmé et parfois reprogrammé par l'utilisateur

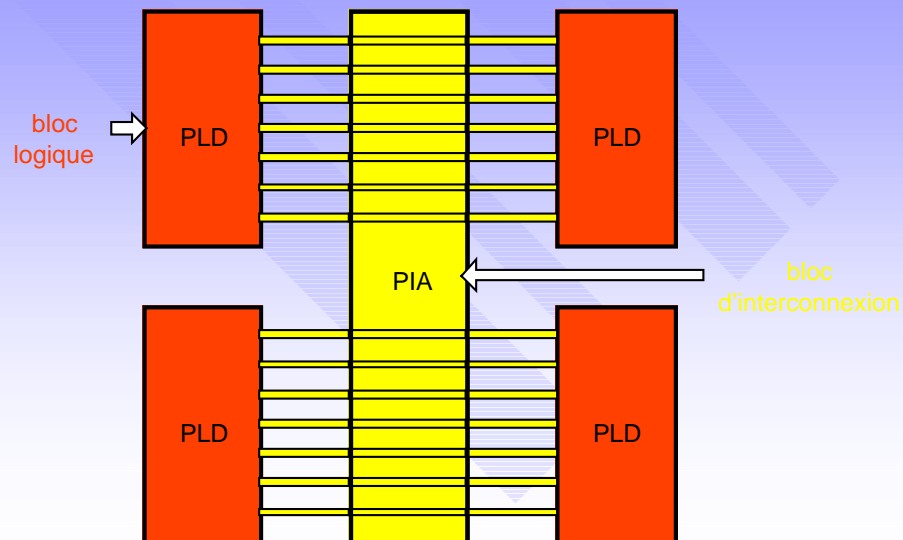
### **Complex Programmable Logic Device (CPLD):**

circuit composé d'un ensemble de blocs logiques tous reliés à un bloc d'interconnexion (Programmable Interconnect Array)

### **Field Programmable Gate Array (FPGA):**

circuit offrant des blocs logiques ainsi que des interconnexions totalement flexibles et qui nécessite un outil de placement-routage

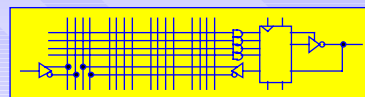
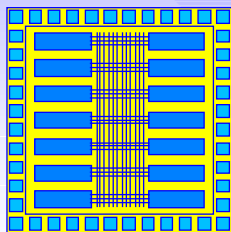
## Complex Programmable Logic Device



## Circuits logiques programmables

### CPLD (Complex Programmable Logic Device):

PLD hiérarchique regroupant un ensemble de circuits GAL (Generic Array Logic) et un réseau d'interconnexion programmable



Implémentation ET-OU-bascule D  
d'une cellule de base d'un circuit GAL



Includes  
MAX 7000E &  
MAX 7000S

# MAX 7000 Programmable Logic Device Family

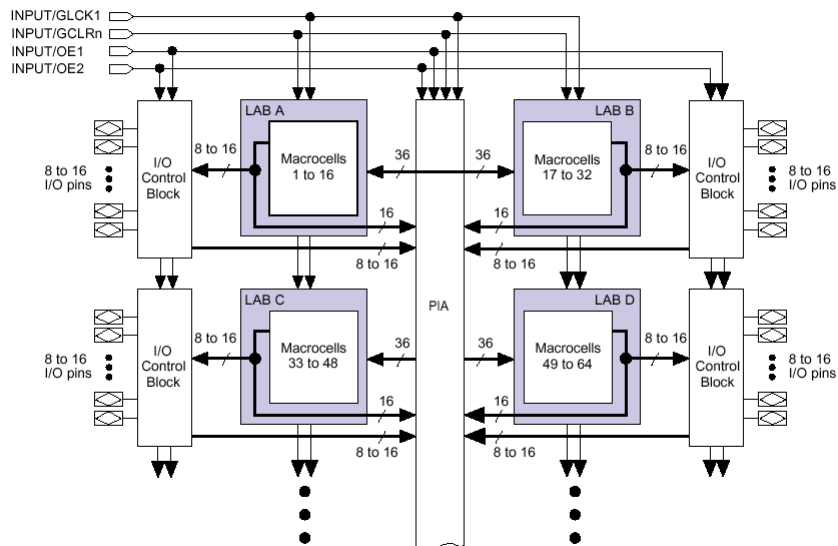
August 2000, ver. 6.02

Data Sheet

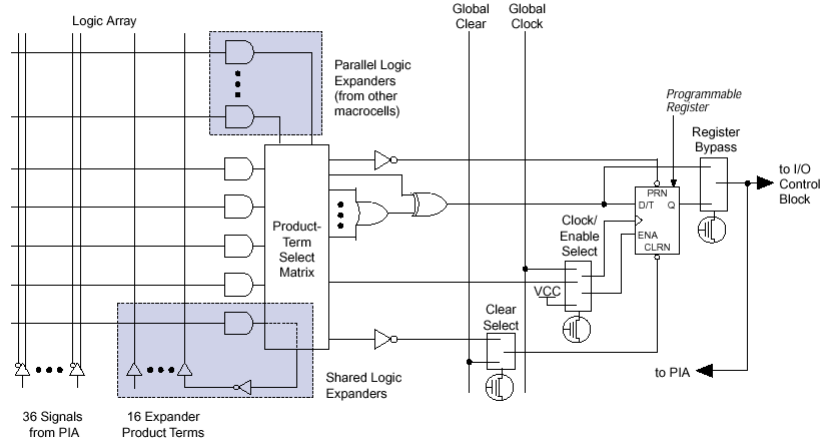
## Features...

- High-performance, EEPROM-based programmable logic devices (PLDs) based on second-generation Multiple Array MatriX (MAX<sup>®</sup>) architecture
- 5.0-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface available in MAX 7000S devices
- Includes 5.0-V MAX 7000 devices and 5.0-V ISP-based MAX 7000S devices
- Built-in JTAG boundary-scan test (BST) circuitry in MAX 7000S devices with 128 or more macrocells
- Complete EPLD family with logic densities ranging from 600 to 5,000 usable gates (see [Tables 1 and 2](#))
- 5-ns pin-to-pin logic delays with up to 175.4-MHz counter frequencies (including interconnect)
- Peripheral component interconnect (PCI)-compliant devices available

Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram



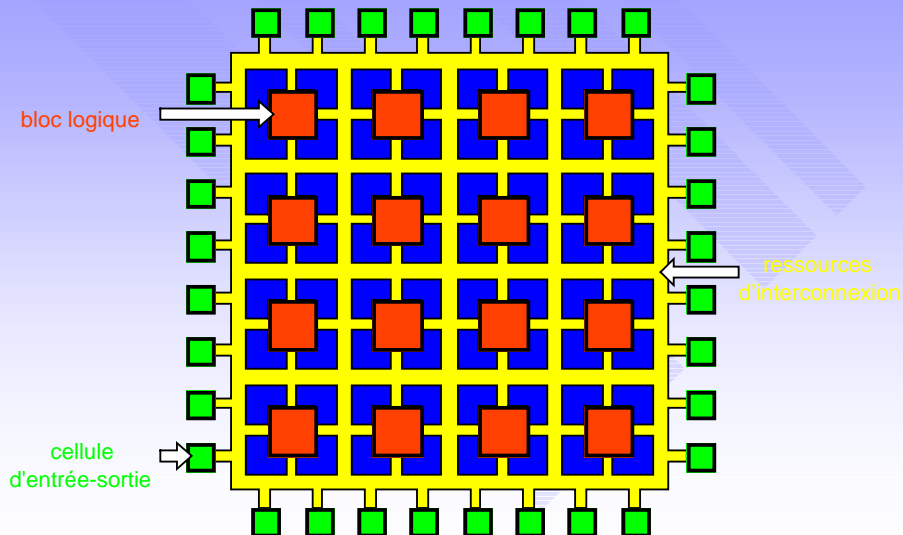
**Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell**



**Table 1. MAX 7000 Device Features**

Feature	EPM7032	EPM7064	EPM7096	EPM7128E	EPM7160E	EPM7192E	EPM7256E
Usable gates	600	1,250	1,800	2,500	3,200	3,750	5,000
Macrocells	32	64	96	128	160	192	256
Logic array blocks	2	4	6	8	10	12	16
Maximum user I/O pins	36	68	76	100	104	124	164
$t_{PD}$ (ns)	6	6	7.5	7.5	10	12	12
$t_{SU}$ (ns)	5	5	6	6	7	7	7
$t_{FSU}$ (ns)	2.5	2.5	3	3	3	3	3
$t_{CO1}$ (ns)	4	4	4.5	4.5	5	6	6
$f_{CNT}$ (MHz)	151.5	151.5	125.0	125.0	100.0	90.9	90.9

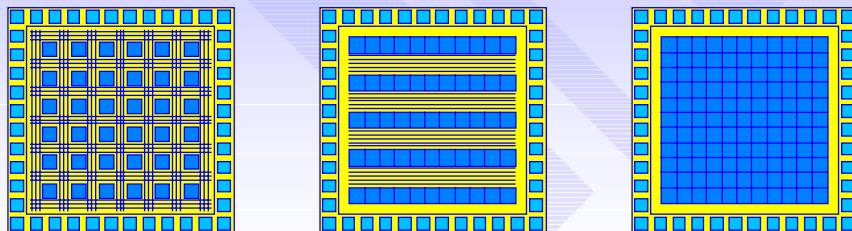
## Field Programmable Gate Array



## Circuits logiques programmables

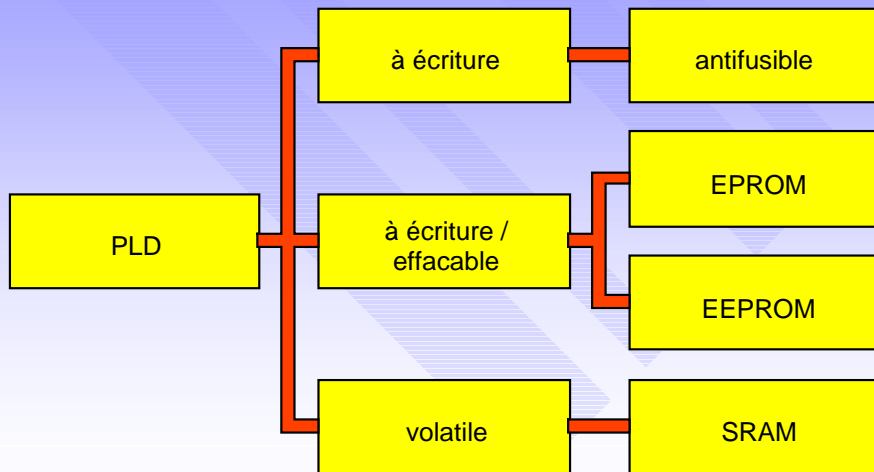
### FPGA (Field-Programmable Gate Array):

réseau de blocs logiques, de cellules d'entrée-sortie et de ressources d'interconnexion; ce réseau est caractérisé par son architecture, sa technologie de programmation et les éléments de base des blocs logiques

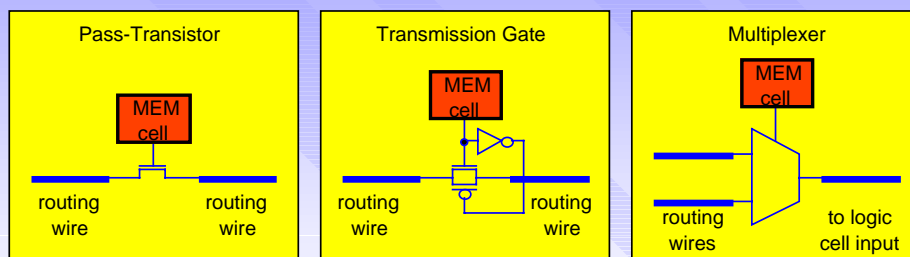


Architectures 2D, row-based et sea of gates

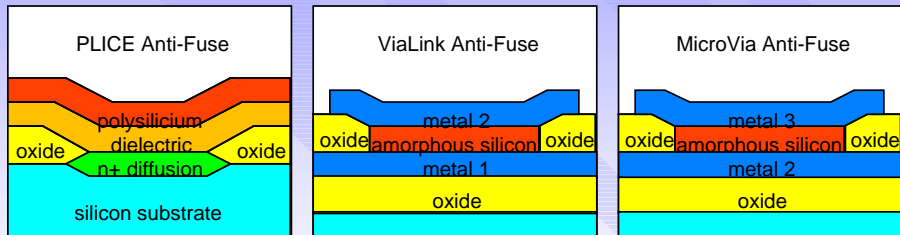
## Technologie de programmation



## Technologie de programmation SRAM, EPROM ou EEPROM



## Technologie de programmation antifusible



## Eléments de base des blocs logiques

paire de transistors	TP
portes logiques de base	AND, XOR
multiplexeurs	MUX
unités fonctionnelles	FU
tables de référence	LUT
basculs bistables	DFF

COMPANY	FAMILY	ARCHITECTURE	LOGIC BLOCK ELEMENTS	PROGRAMMING TECHNOLOGY	EQUIVALENT GATES
XILINX	XC4000 (SPARTAN)	2D array	2(1) x 4(5)in-2(1)out LUT 2 x DFF	SRAM	4K-500K (5K-40K)
XILINX	XC5200	2D array	4 x 4in LUT , 4 x DFF	SRAM	2K-18K
XILINX	XC6200	sea of gates	1 x 2in FU	SRAM	9K-64K
XILINX	XC8100	sea of gates	2in AND - 2in OR (4in AND / DLAT / TBUF)	anti-fuse	1.2K-8.7K
XILINX	VIRTEX (SPARTAN II)	2D array	4 x 4in LUT , 4 x DFF 4 x RAM	SRAM	58K-1.1M 30K-131K bits 15K-150K (16K-48K bits)
ALTERA	FLEX	2D array	8 x 4in LUT , 8 x DFF	SRAM	4K-24K
QUICKLOGIC	pASIC-1	2D array	4 x 2in AND , 2 x 6in AND 1 x 4in MUX , 1 x DFF	anti-fuse	1K-8K
ACTEL	ACT-1	row-based	1 x 4in MUX	anti-fuse	1.2K-2K
ACTEL	ACT-2	row-based	1 x 4in MUX / DFF	anti-fuse	2.5K-8K
ACTEL	ACT-3	row-based	1 x 4in MUX / DFF	anti-fuse	1.5K-10K
CROSSPOINT	CP20K	row-based	4 x TP , 1 x 2in MUX	anti-fuse	1.3K-17K
ATMEL	Cli	sea of gates	3 x 2in AND , 1 x 2in XOR 1 DFF	SRAM	5K



## XC4000E and XC4000X Series Field Programmable Gate Arrays

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May 14, 1999 (Version 1.6)

Product Specification

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### XC4000E and XC4000X Series Features

**Note:** Information in this data sheet covers the XC4000E, XC4000EX, and XC4000XL families. A separate data sheet covers the XC4000XLA and XC4000XV families. Electrical Specifications and package/pin information are covered in separate sections for each family to make the information easier to access, review, and print. For access to these sections, see the Xilinx WebLIXX web site at <http://www.xilinx.com/partinfo/databook.htm#xc4000>.

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Fully PCI compliant (speed grades -2 and faster)
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution

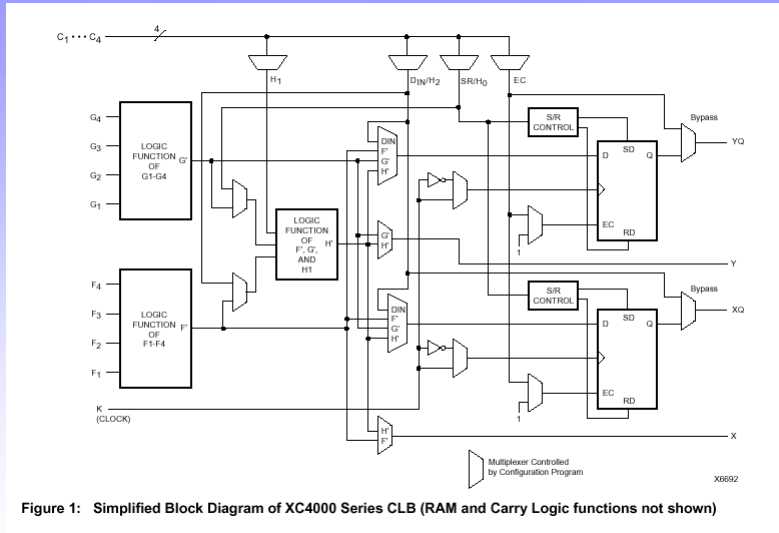
### Low-Voltage Versions Available

- Low-Voltage Devices Function at 3.0 - 3.6 Volts
- XC4000XL: High Performance Low-Voltage Versions of XC4000EX devices

### Additional XC4000X Series Features

- Highest Performance — 3.3 V XC4000XL
- Highest Capacity — Over 180,000 Usable Gates
- 5 V tolerant I/Os on XC4000XL
- 0.35 μm SRAM process for XC4000XL
- Additional Routing Over XC4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
- 12 mA Sink Current Per XC4000X Output
- Flexible New High-Speed Clock Network
  - Eight additional Early Buffers for shorter clock delays
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- Four Additional Address Bits in Master Parallel

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**Table 1: XC4000E and XC4000X Series Field Programmable Gate Arrays**

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O
XC4002XL	152	1,600	2,048	1,000 - 3,000	8 x 8	64	256	64
XC4003E	238	3,000	3,200	2,000 - 5,000	10 x 10	100	360	80
XC4005E/XL	466	5,000	6,272	3,000 - 9,000	14 x 14	196	616	112
XC4006E	608	6,000	8,192	4,000 - 12,000	16 x 16	256	768	128
XC4008E	770	8,000	10,368	6,000 - 15,000	18 x 18	324	936	144
XC4010E/XL	950	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	160
XC4013E/XL	1368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192
XC4020E/XL	1862	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	224
XC4025E	2432	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	256
XC4028EX/XL	2432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256
XC4036EX/XL	3078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288
XC4044XL	3800	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	320
XC4052XL	4598	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	352
XC4062XL	5472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384
XC4085XL	7448	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	448

\* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.