

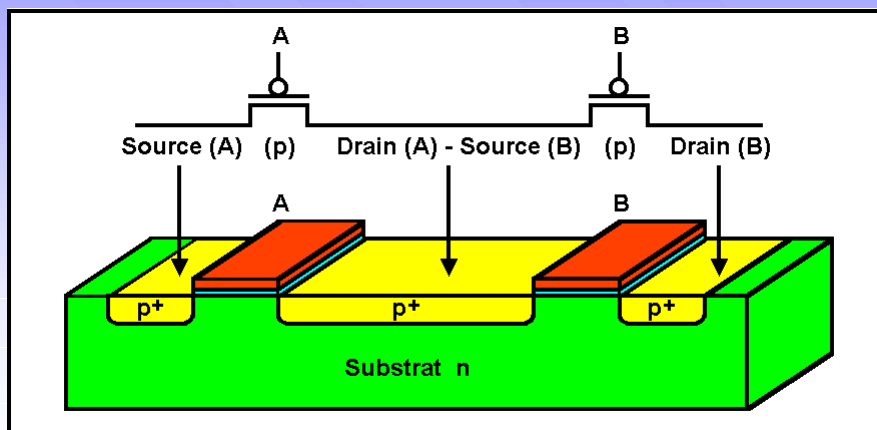
Technologie

- Niveaux de conduction
- Modèle géométrique
- Modèle symbolique

andre.stauffer@epfl.ch

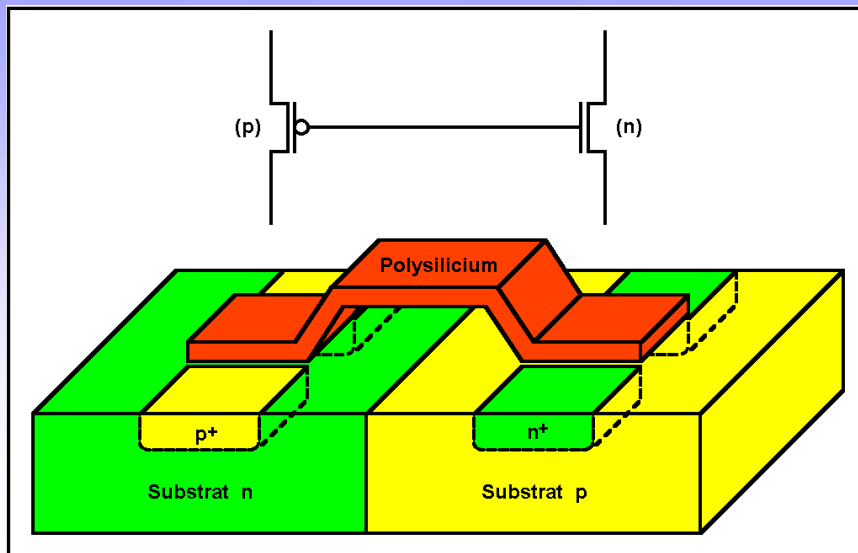
Niveaux de conduction

Premier niveau: la diffusion



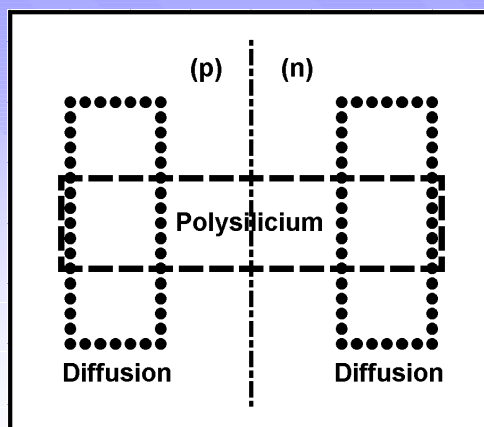
Niveaux de conduction

Second niveau: le polysilicium

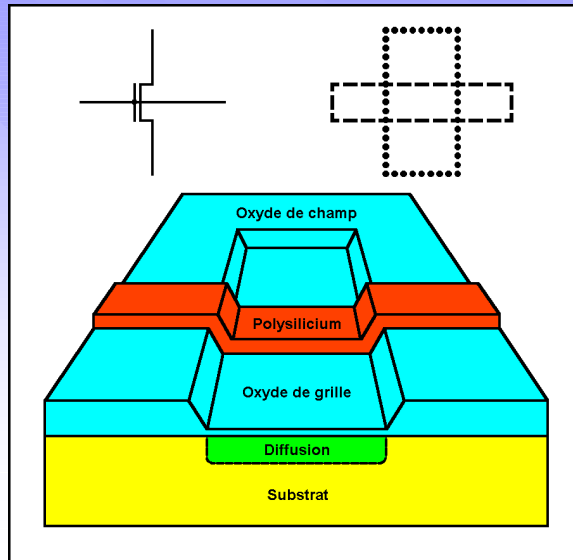


Modèle géométrique

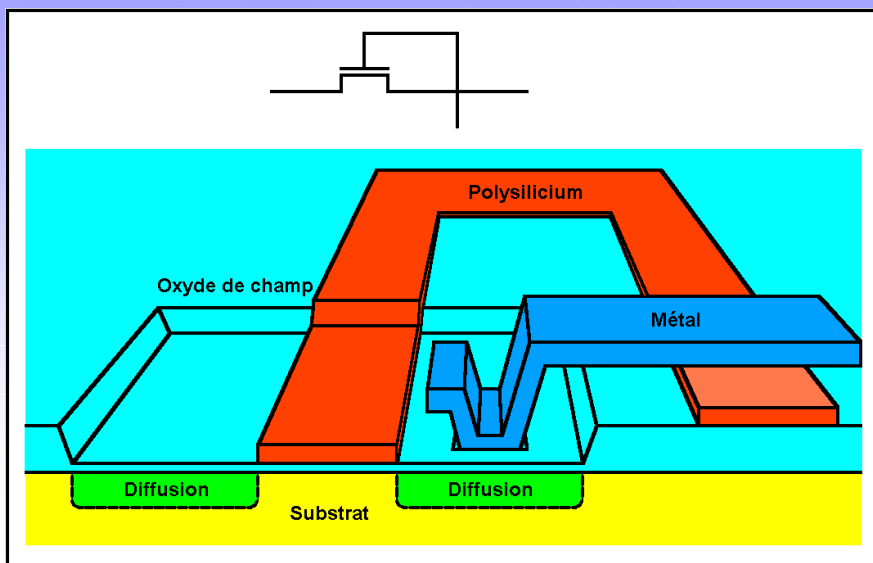
Connexion polysilicium



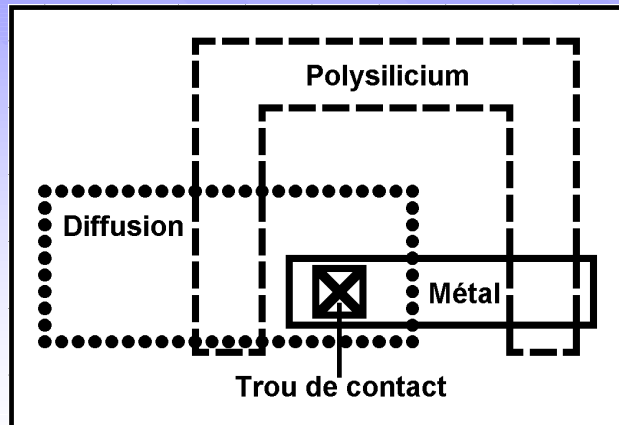
Modèle géométrique Transistor nMOS



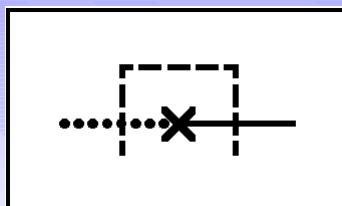
Niveaux de conduction Troisième niveau: le métal



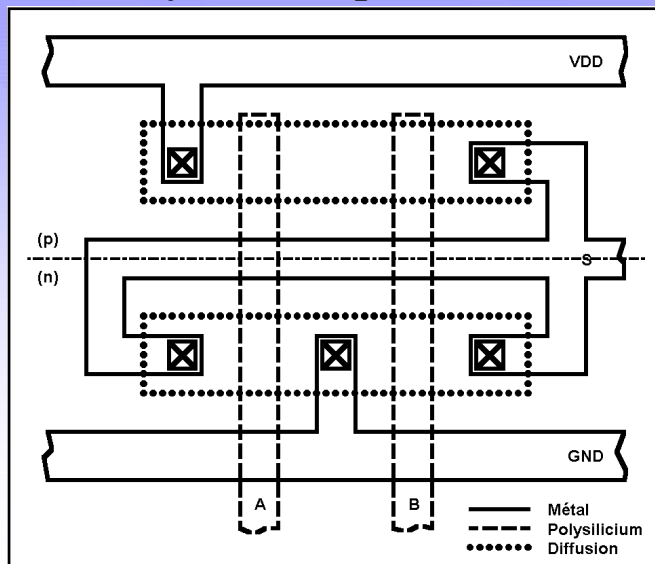
Modèle géométrique Croisement polysilicium-métal



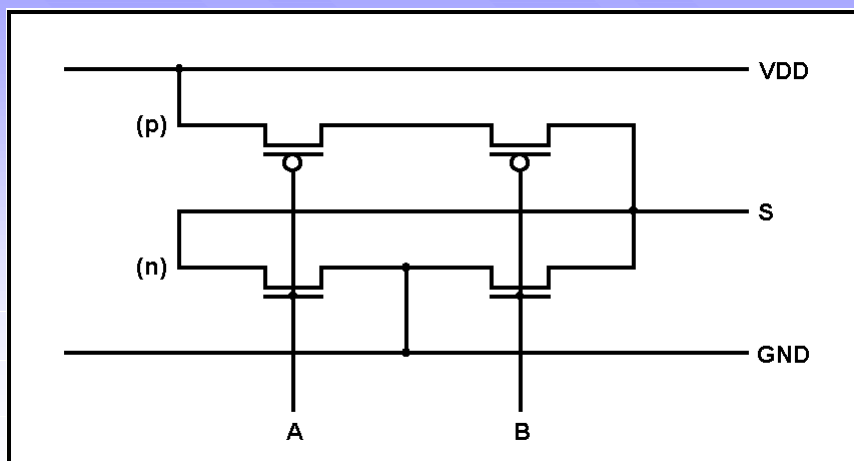
Modèle symbolique Croisement polysilicium-métal



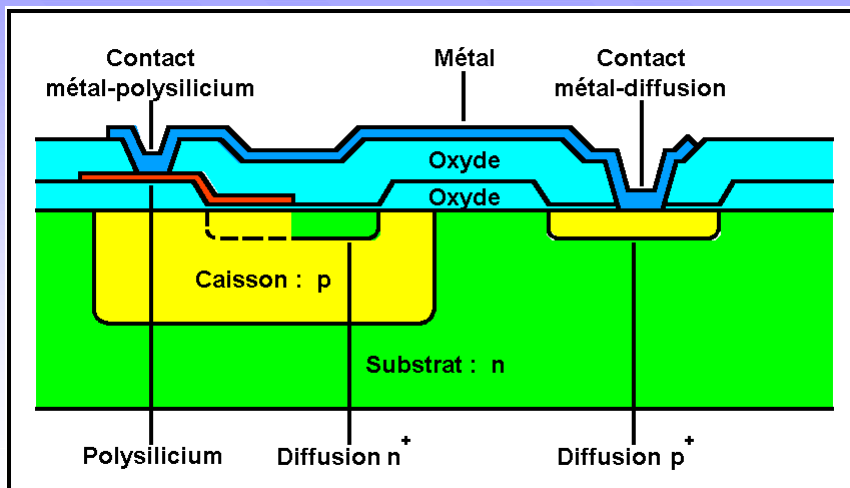
Modèle géométrique Layout de la porte NOR



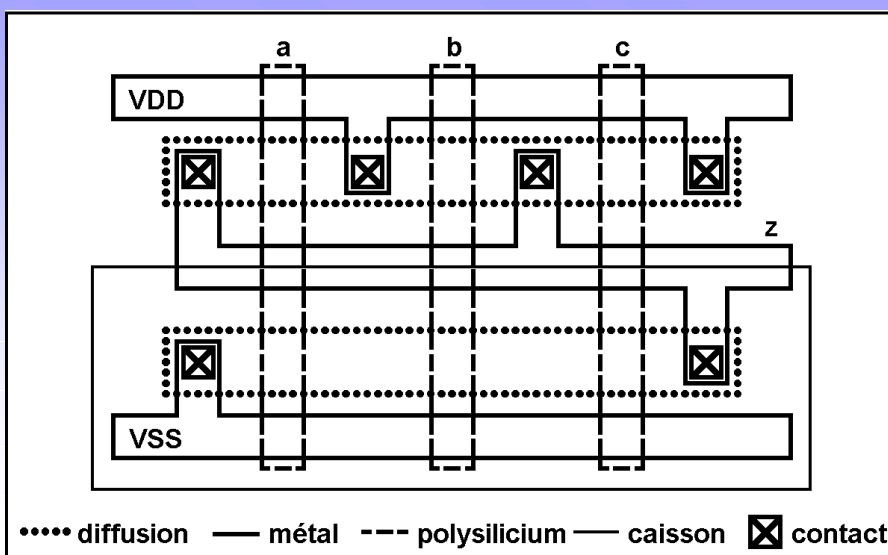
Modèle géométrique Schéma à transistors de la porte NOR



Niveaux de conduction Coupe d'un circuit CMOS

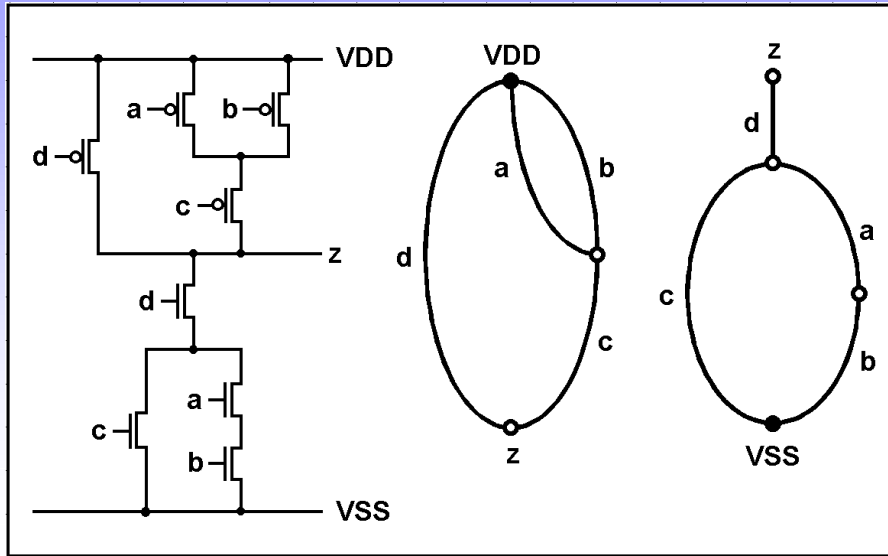


Modèle géométrique Circuit CMOS



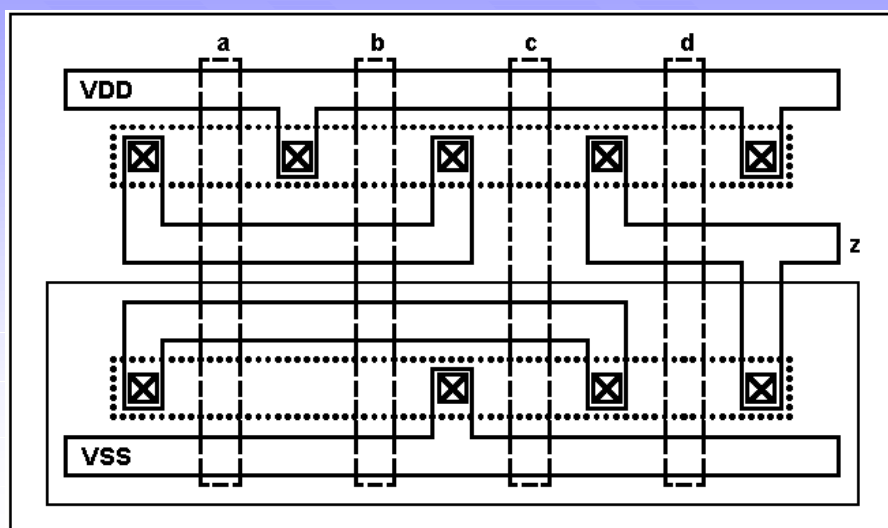
Modèle géométrique

Graphe d'implantation d'une porte CMOS



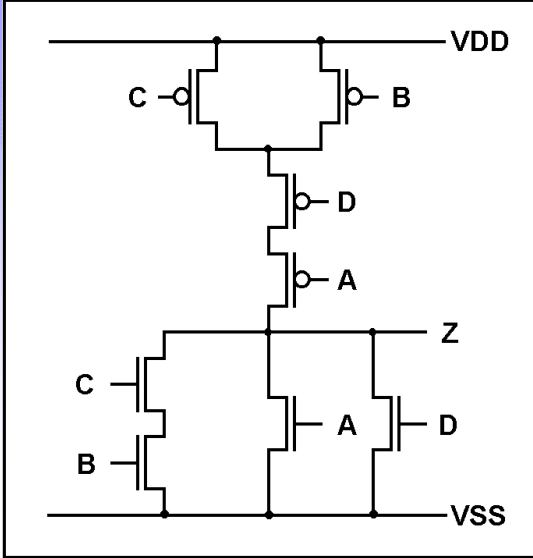
Modèle géométrique

Layout d'une porte CMOS



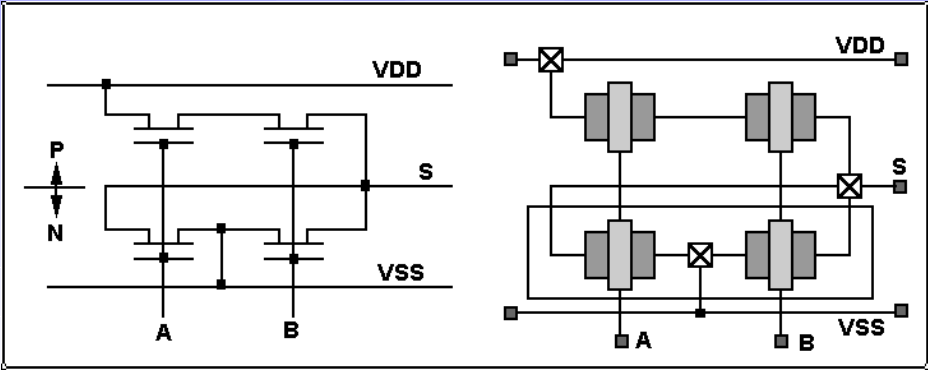
Modèle géométrique

Schéma à transistors



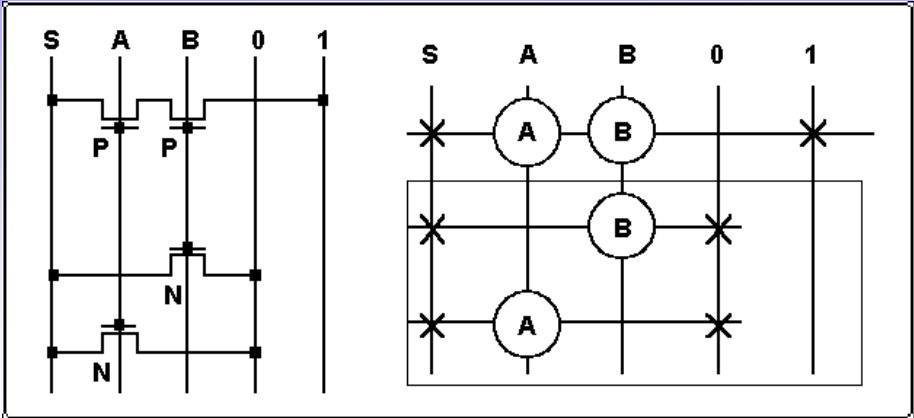
Modèle symbolique

Layout d'une porte NOR



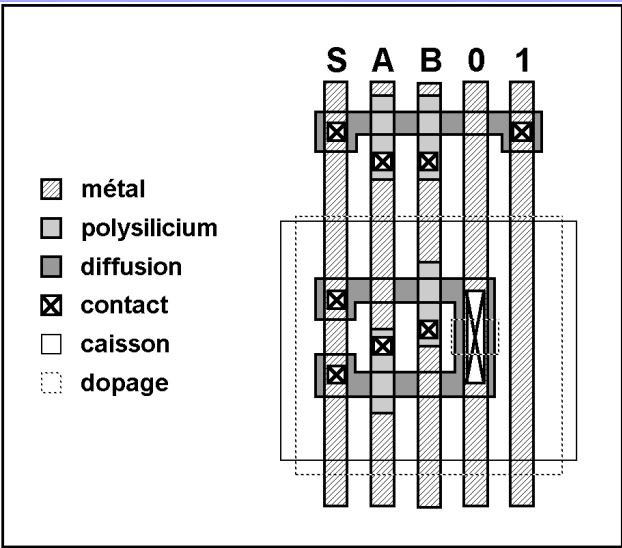
Modèle symbolique

Layout ordonné d'une porte NOR

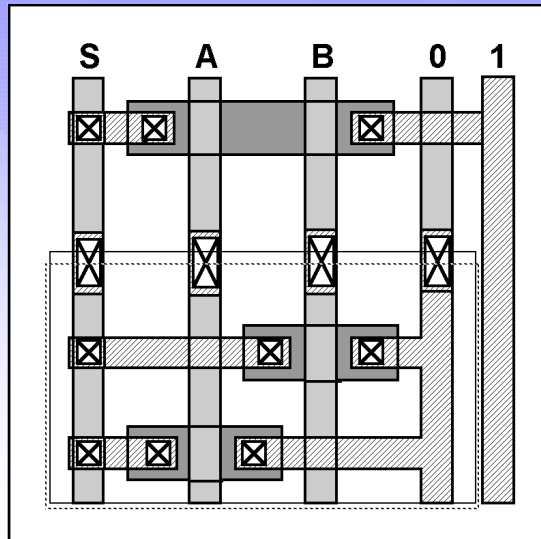


Modèle géométrique

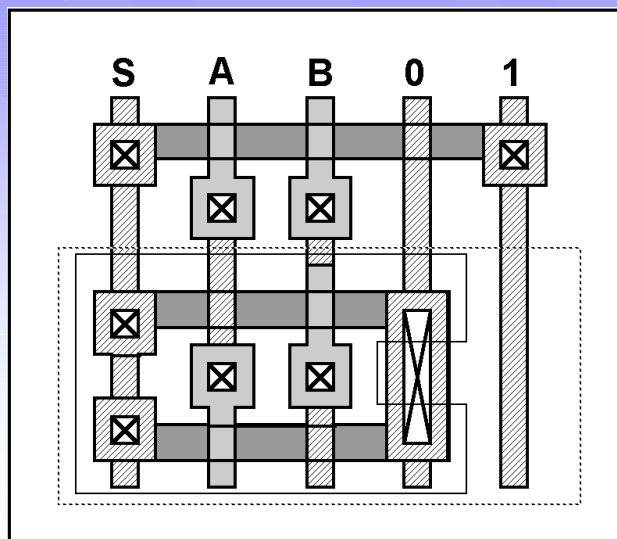
Layout orienté métal (technologie CSEM)



Modèle géométrique Layout orienté poly (technologie CSEM)

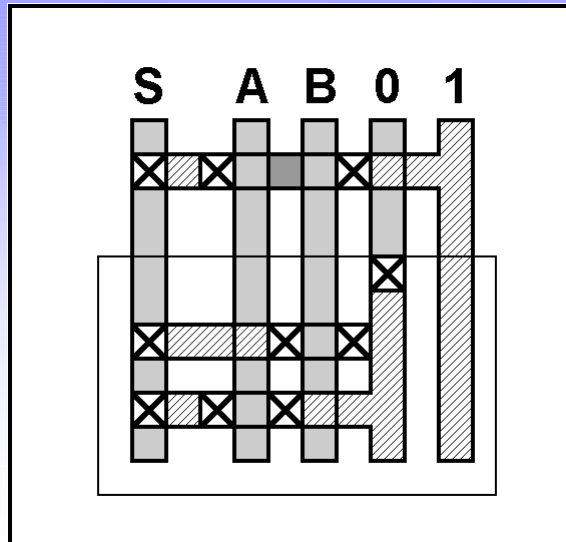


Modèle géométrique Layout orienté métal (technologie MOSIS)



Modèle géométrique

Layout orienté poly (technologie SACMOS)



Modèle géométrique

Layout orienté poly (technologie VLSI)

